DETAILED ACTION

1. This action is in responsive to the application filed on 08/01/2003.

2. Claims 5, 8, 26-33 and 38 have been cancelled.

3. Claims 1-4, 6-7, 9-25, 34-37 and 39-41 are allowed.

EXAMINER'S AMENDMENT

4. An examiner's amendment to the record appear below. Should the change and/or additions be unacceptable to the Applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such amendment, it MUST be submitted no later than the payment of issue fee.

Authorization for examiner's amendment was given in a telephone interview with David P. McAbee, Reg. No. 58,104 on August 12, 2009 to put the case in condition for allowance.

5. The Claims are amended, as presented below, to adopt the changes provided by Applicant's representative on August 12, 2009.

IN THE CLAIMS:

The claim listings below replace all prior versions, and listings, of claims in the application.

Please cancel claims 26-31 and 38 and amend claims 1, 3-4, 6, 11-18, 21, 23 and 34 as follows:

1. (Currently Amended) An apparatus comprising:

a processor including:

marking logic to mark a first speculation identifier associated with ~~instruction information for~~ a[[n]] speculative store instruction of a speculative thread as speculative; and

blocker logic to prevent data associated with the ~~a~~ speculative store instruction of the speculative thread from being forwarded to a non-speculative instruction of a non-speculative thread based on a first address associated with the speculative store instruction and the first speculation identifier in comparison to a second address associated with the non-speculative store instruction and a second speculation identifier associated with ~~information associated with the speculative store instruction of the speculative thread and information associated with~~ the non-speculative instruction ~~of the non-speculative thread.~~ and in response to a first speculation identifier not matching a second speculation identifier.

2. (Original) The apparatus of claim 1, wherein: blocker logic is further to allow the data associated with a store instruction of the speculative thread to be forwarded to an instruction of a second speculative thread.

3. (Currently Amended) The apparatus of claim 1, further comprising: a store request buffer, a store request buffer entry of the store request buffer including a speculation identifier field to hold the first ~~a~~ speculation identifier to indicate the speculative store instruction is speculative and an address field to hold the first ~~an~~ address

~~associated with the store instruction, wherein the information associated with the store instruction includes the speculation identifier and the address.~~

4. (Currently Amended) The apparatus of claim 3, wherein the second speculation identifier is to indicate the non-speculative instruction is non-speculative, and wherein ~~the information associated with the non-speculative instruction of the non-speculative thread includes a second speculation identifier to indicate the non-speculative instruction is non-speculative thread and a second address associated with the non-speculative instruction, and wherein~~ blocker logic to prevent data associated with the speculative store instruction from being forwarded to the non-speculative instruction based on ~~the speculation identifier, the address, the second address, and the second speculation identifier comprises: blocker logic to prevent data associated with the speculative store instruction from being forwarded to the non-speculative instruction in response to a comparison of a first combination of the speculative identifier and the address not matching a second combination of the second speculative identifier and the second address.~~ a first address associated with the speculative store instruction and the first speculation identifier in comparison to a second address associated with the non-speculative store instruction and a second speculation identifier associated with the non-speculative instruction comprises the blocker logic to compare a first combination of the first address and the first speculation identifier with a second combination of the second address and the second speculation identifier and to determine the first combination is different from the second combination based on the first speculation identifier and the second speculation identifier being different.

5. (Cancelled)

6. (Currently Amended) The apparatus of claim 1, wherein blocker logic further includes:

dependence blocker logic to prevent the data associated with the ~~a~~ speculative store instruction from being forwarded to the non-speculative ~~an~~ instruction of the non-speculative thread ~~based on information associated with the store instruction of the speculative thread and information associated with the non-speculative thread~~; and

store blocker logic to prevent the data from being stored in a memory system.

7. (Previously Amended) The apparatus of claim 6, wherein: store blocker logic is outside an execution pipeline.

8. (Cancelled)

9. (Original) The apparatus of claim 6, wherein: dependence blocker logic is included in an execution pipeline.

10. (Previously Amended) The apparatus of claim 9, wherein: dependence blocker logic is included in a memory ordering buffer of the processor.

11. (Currently Amended) A system, comprising:

a memory system that includes a memory device; and

a processor associated with the memory system, the processor including dependence blocker logic to prevent data associated with a store instruction of a speculative thread from being forwarded to a[[n]] non-speculative instruction of a non-speculative thread in response to a first speculation identifier associated with the store instruction not matching a second speculation identifier associated with the non-speculative instruction ~~without replacement of the instruction of the non-speculative thread,~~ based on a first address associated with the speculative store instruction and the first

speculation identifier in comparison to a second address associated with the non-speculative instruction and the second speculation identifier associated with the non-speculative instruction and to allow the data associated with the store instruction of the speculative thread to be forwarded to a speculative instruction of another speculative thread in response to the first speculation identifier matching a third speculation identifier associated with the speculative instruction.

12. (Currently Amended) The system of claim 11, wherein: the processor further includes store blocker logic to prevent the data from being stored in the memory system and marking logic to mark the first and the third speculation identifiers ~~instruction information associated with the store instruction~~ as speculative.

13. (Currently Amended) The system of claim 12, wherein: the first, second, and third speculation identifiers (IDs) include ~~marking logic is further to associate a~~ safe speculation domain IDs ~~with the instruction information~~.

14. (Currently Amended) The system of claim 13, wherein: the first safe speculation domain ID includes a first thread identifier to identify the speculative thread associated with the store instruction, the second safe speculation domain ID includes a second thread identifier to identify the non-speculative thread associated with the non-speculative instruction, and the third safe speculation domain ID includes a third thread identifier to identify the another speculative thread associated with the speculative instruction. ~~the marking logic is further to indicate a thread identifier as the speculation domain ID.~~

15. (Currently Amended) The system of claim 12, further comprising: a store request buffer to store the first speculation ~~domain~~ ID.

16. (Currently Amended) The system of claim 11, wherein: the processor includes a first logical processor to execute the non-speculative thread[[; and the processor includes]] a second logical processor to execute the speculative thread, and a third logical processor to execute the another speculative thread.

17. (Currently Amended) The system of claim 11, further comprising: a second processor ~~that includes said dependence blocker logic and said store blocker logic;~~ wherein the ~~said~~ processor is to execute the non-speculative thread, the ~~and said~~ second processor is to execute the speculative thread, and the second processor is to execution the another speculative thread.

18. (Currently Amended) The system of claim of claim 11, wherein: the memory system includes store blocker logic to prevent the data from being stored in the memory system in response to a first speculation identifier associated with the store instruction not matching a second speculation identifier associated with the non-speculative instruction and a cache organized to include a plurality of tag lines, wherein each tag line of the cache includes a unique helper thread ID field.

19. (Original) The system of claim 11, wherein: the memory system includes a cache organized to include a plurality of tag lines, wherein each tag line of the cache includes a safe-store indicator field.

20. (Original) The system of claim 11, wherein: the memory system includes a victim tag cache to indicate evicted cache lines that include speculative load data.

21. (Currently Amended) A method, comprising:

receiving instruction information for a load instruction, the instruction information including a load address;

performing a dependence check, wherein performing the dependence check includes:

determining if a store address of an in-flight store instruction matches the load address; and

determining if the load instruction and the in-flight store instruction each originate with a speculative thread based on a first speculation identifier associated with the in-flight store instruction and a second speculation identifier associated with the load instruction;

determining the dependence check is successful in response to determining the store address matches the load address and determining the load instruction and the in-flight store instruction each originate with a speculative thread;

forwarding, if the dependence check is successful, store data associated with the in-flight store instruction to the load instruction; and

declining to forward the store data to the load instruction, if the dependence check is not successful in response to a first speculation identifier not matching a second speculation identifier, ~~the store data to the load instruction.~~

22. (Original) The method of claim 21, wherein performing the dependence check further comprises: determining if the in-flight store instruction and the load instruction originate from the same thread.

23. (Currently Amended) The method of claim 22, wherein determining if the in-flight store instruction and the load instruction originate from the same thread further comprises: determining if a thread ID included in the first speculation identifier ~~associated with the in-flight store instruction~~ matches a thread ID included in the second speculation identifier ~~associated with the load instruction~~.

24. (Original) The method of claim 21, wherein performing the dependence check further comprises: if the load instruction and the in-flight store instruction do not each originate with a speculative thread, determining if the load instruction and the in-flight store instruction each originate with a non-speculative thread.

25. (Original) The method of claim 21, further wherein: declining to forward further comprises declining to forward the store data to the load instruction if (the load instruction and the in-flight store instruction each originate with a speculative thread) AND (the in-flight store instruction originates with a speculative thread that is not older in program order than the speculative thread from which the load instruction originates).

26. (Cancelled)

27. (Cancelled)

28. (Cancelled)

29. (Cancelled)

30. (Cancelled)

31. (Cancelled)

32. (Cancelled)

33. (Cancelled)

34. (Currently Amended) An apparatus comprising:

a processor including:

a first logical processor to execute a speculative thread;

a second logical processor to execute a non-speculative thread;

a storage area to include a speculation identifier (ID) field, the speculation ID field to hold a first value to indicate an associated store instruction is associated with the speculative thread; and

control logic to prevent data associated with the store instruction from being consumed by the non-speculative thread, based on the speculation ID holding the first value[[.]] wherein: the control logic includes comparison logic to compare a second address and a second ID value, which are associated with a load instruction that is to be executed as part of the non- speculative thread on the second logical processor, with the first address and the first ID value; and store blocker logic to prevent data associated with the store instruction from being consumed by the load instruction that is to be executed as part of the non-speculative thread, in response to the first ID value and the first address not matching the second ID value and the second address.

35. (Previously Added) The apparatus of claim 34, wherein: the first and the second logical processors are the same logical processor, and wherein the non-speculative thread and the speculative thread are to be time multiplexed for execution on the same logical processor.

36. (Previously Added) The apparatus of claim 34, wherein: the storage area includes a store buffer, and wherein the speculation ID field is included within a store buffer entry of the store buffer, the store buffer entry to also hold a first address associated with the store instruction and the data associated with the store instruction.

37. (Previously Added) The apparatus of claim 36, wherein: the first value is to include a first identifier (ID) value associated with the first logical processor.

38. (Cancelled)

39. (Previously Added) The apparatus of claim 34, wherein: the processor further includes a third logical processor to execute an additional speculative thread, and wherein the control logic is to allow data associated with the store instruction from being consumed by the additional speculative thread.

40. (Currently Amended) The apparatus of claim 34, wherein: the first value is to include a 1-bit mode value.

~~comparison logic.~~

41. (Previously Added) The apparatus of claim 34, wherein: the processor further includes marking logic to set the speculation ID field to the first value in response to detecting the store instruction associated with the speculative thread.

--End--

Allowable Subject Matter

6. The following is an examiner's statement of reasons for allowance:

As applicant pointed out under Remark section, pages 16-18, Chamdani et al. (US 2004/0073906 A1), taken either singly and/or in combination with other cited prior arts, do not teach the combined functional limitations of blocker logic or control logic to prevent data associated with the speculative store instruction of the speculative thread from being forwarded to a non-speculative instruction of a non-speculative thread based on a first address associated with the speculative store instruction and the first speculation identifier in comparison to a second address associated with the non-speculative store instruction and a second speculation identifier associated with the non-speculative instruction and in response to a first speculation identifier not matching a second speculation identifier, as recited in such manners in each of independent claims 1, 11, 21 and 34.

Prior arts of record do not teach and/or suggest these claimed limitations, thus, all remaining pending claims 1-4, 6-7, 9-25, 34-37 and 39-41 are allowed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ISAAC T. TECKLU whose telephone number is (571) 272-7957. The examiner can normally be reached on M-TH 9:300A - 8:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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